

AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): A method of fabricating
a ~~low temperature polysilicon (LTPS)~~ thin film
5 transistor (TFT), ~~the method comprising following~~
~~steps:~~

providing a substrate;
forming a polysilicon film on the substrate, the
polysilicon film defined with a source region,
10 a drain region, and a channel region between the
source region and the drain region;
forming a gate insulating layer ~~on~~ above the
substrate;
forming a gate ~~on~~ above the substrate;
15 performing an ion implantation process to form a
source in the source region and a drain in the
drain region;
forming a silane based silicon nitride layer
covering the gate and the polysilicon film; and
20 forming a TEOS based silicon oxide layer on the
silicon nitride layer.

Claim 2 (currently amended): The method of claim 1
further comprising following steps:
25 performing a photo-etching process to form a
contact hole on the source and ~~another contact~~
~~hole on the drain~~ respectively; and
filling a conductive layer in the contact holes,
the conductive layer being electrically
30 connected to the source and the drain.

Claim 3 (original): The method of claim 1 wherein the

method of forming the polysilicon film comprises
following steps:

- forming an amorphous silicon film on the substrate;
and
- 5 performing an excimer laser annealing process to
make the amorphous silicon film crystallize to
the polysilicon film.

Claim 4 (cancelled)

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Claim 5 (original): The method of claim 4 wherein the
silicon nitride layer comprises 20% to 40% hydrogen
atoms and serves as a hydrogen source of a
hydrogenating process.

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Claim 6 (original): The method of claim 1 wherein the
gate is a metal gate.

Claim 7 (currently amended): The method of claim 1
20 wherein the silicon oxide has a thickness in a range
of ~~2500~~500 to 10000 angstroms.

Claim 8 (currently amended): The method of claim 1
wherein the silicon nitride has a thickness in a range
25 of 500 to ~~3500~~5000 angstroms.

Claim 9 (original): The method of claim 1 wherein the
method forms the silicon nitride layer by performing
a first plasma enhanced chemical vapor deposition
30 (PECVD) process.

Claim 10 (original): The method of claim 9 wherein the

method forms the silicon oxide layer by performing a second plasma enhanced chemical vapor deposition process.

5 Claim 11 (currently amended): The method of claim 10 wherein the first PECVD process and the second PECVD process are performed in the same ~~reacting~~ chamber.

10 Claim 12 (currently amended): The method of claim 10 wherein the first PECVD process and the second PECVD process are performed in different ~~reacting~~ chambers.

15 Claim 13 (original): The method of claim 1 wherein the low temperature polysilicon thin film transistor is a top gate low temperature polysilicon thin film transistor or a bottom gate low temperature polysilicon thin film transistor.